===

Summary of some aspects of the
Workshop on Bump Bonding and Die Attach Technologies
held at CERN on June 11-12 2003

Dylan Walker, SUNY Stony Brook
Johann M. Heuser, RIKEN

===

The purpose of the workshop, summarized by Ch. Joram, was to discuss status, techniques and problems of industrial interconnection technologies, which are essential for current and near future detector construction projects in high energy and nuclear physics.
The program, the participants from industry, experimental physics community and technical services, as well as links to the presentations, are accessible through the workshop's webpage: http://cern.ch/ssd/bond

While several talks reviewed basic bonding technologies, most of the presentations were specific to particular detector applications. We overview here the status of two basic interconnection technologies: wire bonding and bump bonding.

Wire bonding:

- A general introduction to wire bonding was given by Josef Sedlmair from Delvotec company, Germany.

- Wire-bonding uses the technique of friction-welding to establish micro-electrical connections e.g., between sensors and read-out chips.
    - Accomplished through the application of ultrasonic vibrations while subjecting wire ends to pressure.

- Advantages/Disadvantages:
    - A variety of diverse materials can be bonded.
    - Unlike ordinary welding, the bond is thermodynamically meta-stable.

- Characteristics:
    - Typically materials of similar hardness and roughness are bonded.
    - ~95% of all bonds are Au (handled under heat – mostly in industry)
    - ~5% Al (at room temperature – usually chosen for physics applications).
    - Cu (difficult because of oxidation problem) and other exotic materials under study.
    - Wire diameter (typical 17-75 um)
    - Pad material (e.g. gold, aluminum), thickness up to few microns.

- Most common: wedge bonding technique; typically
  - 1st bond on chip
  - 2nd bond on circuit board

- Metallurgy for wire-bonding was explained in a talk by Rui De Oliveira, mainly describing gold and aluminum based techniques, and different plating processes.

- Bond parameters:
  - frequency (~60-140 kHz)
  - welding time (~5-30 ms)
  - bond force (several grams to tens of grams)
  - loop parameters
  - pitch (> 35 um) and length of bond (~0.5-4 mm)

- To Avoid Pitfalls:
  - Ian McGill gave an overview on common problems in design and execution.
  - Choose layout compatible with bond technology.
  - Cleanliness and homogeneous, consistent structure and quality of surfaces required for strong and stable bonds.
  - Controlled storage/transportation environment before/after bonding
  - Thorough prototyping and development of specific tools before a "mass production".

- A truly large-scale application of wire-bonding was discussed by Alan Honma for the CMS silicon tracker.

Bump bonding:
- Bump bonding is a process by which a connection between two components (e.g, readout chip and sensor) is established. Small solder balls ("bumps") are deposited on one wafer with associated solderable pads on the other. The two components are then aligned and brought together ("bonded") through a flip chip process.

- Bump bonding and Flip Chip Interconnection for silicon pixel detector projects at CERN was introduced and reviewd by Michael Campbell.

- Jorma Salmi of VTT, Finland, gave a general overview of their bump bonding process.

- Characteristics:
  - Pitch (~50 um)
  - Bumps/chip (~1,000-10,000)
  - Sn-Pb alloy for bumps provides mechanical strength
  - wafer thinning (back-grinding) can be performed after bump deposition on the electronics wafer, before the flip chipping is done.

- Flip chip process:
    - prelim alignment, laser autocollinator, and lateral alignment
    - heating of chips w/ infrared halogen
    - compression of heat-softened bumps
    - reflow bonding
    - cooling

- The application of this technology for the ALICE silicon pixel detector was reviewed by Petra Riedler. Another approach for ALICE uses Indium bumps from AMS, Italy.

- An alternative bump bond technology has been developed at the Paul Scherrer Institute for the CMS pixel detector. It uses indium bumps that are placed on the chips with an in-house developed machine. This setup was reviewed by Stefan Heising.